IN THE UNITED STATES DISTRICT COURT
FOR THE NORTHERN DISTRICT OF TEXAS
DALLAS DIVISION

COMPLEX MEMORY, LLC, Plaintiff -against- STMICROELECTRONICS, INC., Defendant	Civil Action No.: 3:18-cv-3018 **Jury Trial Demanded**

COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff Complex Memory, LLC ("Complex Memory"), by way of this Complaint against Defendant STMicroelectronics, Inc. ("STM") ("Defendant" or "STM" herein), alleges as follows:

PARTIES

1. Plaintiff Complex Memory is a limited liability company organized and existing under the laws of the State of Texas, having its principal place of business at 7116 Nicki Court, Dallas, Texas 75252.

2. On information and belief, Defendant STM is a Delaware corporation, with headquarters at 750 Canyon Drive, Suite 300, Coppell, TX 75019.

JURISDICTION AND VENUE

3. This is an action under the patent laws of the United States, 35 U.S.C. §§ 1, *et seq.*, for infringement by STM of claims of U.S. Patent Nos. 5,890,195; 5,896,550; 5,963,481; and 6,658,576; ("the Patents-in-Suit").

4. This Court has subject matter jurisdiction pursuant to 28 U.S.C. §§ 1331 and 1338(a).

5. STM is subject to the personal jurisdiction of this Court because, *inter alia*, on information and belief, (i) STM is registered to transact business in the State of Texas; (ii) STM is headquartered in the State of the Texas; and (iii) STM has committed and continues to commit acts of patent infringement in the State of Texas, including by making, using, offering to sell, and/or selling accused products and services in Texas, and/or importing accused products and services into Texas. In addition, or in the alternative, this Court has personal jurisdiction over STM pursuant to Fed. R. Civ. P. 4(k)(2).

6. Venue is proper as to STM in this district under 28 U.S.C. § 1400(b) because, *inter alia*, on information and belief, STM has a regular and established place of business in this district and has committed and continues to commit acts of patent infringement in the State of Texas, including by making, using, offering to sell, and/or selling accused products and services into the State of Texas, and/or importing accused products and services into the State of Texas.

BACKGROUND

7. On March 30, 1999, the United States Patent and Trademark Office duly and lawfully issued U.S. Patent No. 5,890,195 ("the '195 Patent"), entitled "DRAM With Integral SRAM Comprising A Plurality Of Sets Of Address Latches Each Associated With One Of A Plurality Of SRAM." A copy of the '195 Patent is attached as Exhibit A.

8. G.R. Mohan Rao invented the technology claimed in the '195 Patent.

9. On April 20, 1999, the United States Patent and Trademark Office duly and lawfully issued U.S. Patent No. 5,896,550 ("the '550 Patent"), entitled "Direct Memory Access Controller With Full Read/Write Capability." A copy of the '550 Patent is attached as Exhibit B.

10. Omer Lem Wehunt and Jeffrey M. Lavin invented the technology claimed in the '550 Patent.

11. On October 5, 1999, the United States Patent and Trademark Office duly and lawfully issued U.S. Patent No. 5,963,481 ("the '481 Patent"), entitled "Embedded Enhanced DRAM, And Associated Method." A copy of the '481 Patent is attached as Exhibit C.

12. Michael Alwais and Michael Peters invented the technology claimed in the '481 Patent.

13. On December 2, 2003, the United States Patent and Trademark Office duly and lawfully issued U.S. Patent No. 6,658,576 ("the '576 Patent"), entitled "Energy-Conserving Communication Apparatus Selectively Switching Between A Main Processor With Main Operating Instructions And Keep-Alive Processor With Keep-Alive Operating Instruction." A copy of the '576 Patent is attached as Exhibit D.

14. Howard Hong-Dough Lee invented the technology claimed in the '576 Patent.

15. Complex Memory is the assignee and owner of the right, title, and interest in and to the Patents-in-Suit, including the right to assert all causes of action arising under said patents and the right to any remedies for infringement.

NOTICE

16. By letter dated April 12, 2018, Complex Memory notified STM of the existence of the Patents-in-Suit, and of infringement thereof by STM and its customers. Complex Memory's letter identified exemplary infringing STM products and an exemplary infringed claim for each of the Patents-in-Suit.

17. In addition, while prosecuting U.S. Patent Application No. 09/411,617, which matured into U.S. Patent No. 6,298,394, STM notified the U.S. Patent and Trademark Office of the existence of the '550 Patent.

18. By letter dated May 1, 2018, STM acknowledged receipt of Complex Memory's April 12, 2018 letter but stated that it "intends to take no further action with regard to this matter."

19. Accordingly, STM has received notice of the Patents-in-Suit and of infringement thereof

by STM and its customers.

COUNT I: INFRINGEMENT OF THE '195 PATENT

20. Plaintiff incorporates the preceding paragraphs as if fully set forth herein.

21. On information and belief, STM has infringed the '195 Patent pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, offering to sell, selling in the United States or importing into the United States the devices identified in Attachment A ("Accused STM Products").

22. For example, on information and belief, STM has infringed at least claim 6 of the '195 Patent by performing a method of accessing blocks of data in a memory having a plurality of registers and a memory array. For example, the Accused STM Products include STM's STiH platform, including the STiH416 model. On information and belief, the STiH platform includes an ARM Cortex-A9 Core, including L1 and L2 cache memories having a plurality of registers and a memory array. *See, e.g.,* Ex. 1, STiH416 Datasheet. *See also* Ex. 2, ARM Cortex-A Series Programmer's Guide Version 4.0, Chapter 8.4.1 Cache terminology. In performing the method of claim 6, a processing core received an address through an address port such as an address input to a cache controller (*See* Ex. 3, ARM Cortex-A Series Programmer's Guide Version 4.0, Chapter 8.4.5 Cache controller) or an address channel of a bus. The Accused STM Products compared the received address with addresses previously stored in each of a plurality of latches, such as the latches holding addresses stored in cache memory. "When it receives a request from the core it must check to see whether the requested address is to be found in the cache. This is known as a cache look-up. It does this by comparing a subset of the address bits of the request with tag values associated with lines in the cache." *Id.,* Ex. 3, ARM Cortex-A Series Programmer's Guide Version 4.0, Chapter 8.4.5 Cache controller. When a match between the

received address and a matching address stored in a one of the latches occurred, the Accused STM Products performed the substep of accessing a register corresponding to the latches storing the matching address through a data port. "If there is a match (a hit) and the line is marked valid then the read or write will happen using the cache memory." *Id.* When a match between the received address and an address stored in one of the latches did not occur, the Accused STM Products performed the substeps of exchanging data between a location in the memory array addressed by the received address and a selected one of the registers. "Whenever the core wants to read or write a particular address, it will first look for it in the cache. If it finds the address in the cache, it will use the data in the cache, rather than having to perform an access to main memory." Ex. 4, ARM Cortex-A Series Programmer's Guide Version 4.0, Chapter 8 Caches. When the match did not occur, the Accused STM Products further stored the received address in one of the latches corresponding to the selected register. For example, the Accused STM Products stored the received address, such as the tag, corresponding to the register being accessed, in the cache memory system registers, including in the TAG RAM, address status and data bits, and in way, index, and tag registers, such as the current TAG, set, index, and way registers. *See* Ex. 2, ARM Cortex-A Series Programmer's Guide Version 4.0, Chapter 8.4.1 Cache terminology. The Accused STM Products further modified the received address to generate a modified address. For example, the hardware in the Accused STM Products prefetches, for example, data stored at one or more prefetch addresses by modifying the address received by the processor for memory access. *See* Ex. 5 Cortex-A9 Revision: r4p1 Technical Reference Manual, Chapter 7.6.2 Data prefetching. *See also* Ex. 6 ARM Cortex-A15 MPCore Processor Technical Reference Manual, Chapter 7.4, L2 cache prefetcher ("[P]refetch address = current address + (stride x programmed distance."). On information and belief, the Accused

STM Products also modify the received address during a speculative lookup, including for speculative TAG lookup and speculative linefills. The Accused STM Products further exchanged data between a location in the memory array addressed by the modified address and a second selected one of the registers. For example, "Whenever the core wants to read or write a particular address, it will first look for it in the cache. If it finds the address in the cache, it will use the data in the cache, rather than having to perform an access to main memory." *See* Ex. 4 ARM Cortex-A Series Programmer's Guide Version 4.0, Chapter 8 Caches. The Accused STM Products then stored the modified address in of one of the latches corresponding to the second selected register. For example, during the hardware prefetch, in connection with the prefetched data being loaded into the cache, the processor stored the modified address and/or tag in the latches storing addresses, including in the TAG RAM, address status and data bits, and in way, index, and tag registers, such as the current TAG, set, index, and way registers.

23. On information and belief, STM has committed the foregoing infringing activities without a license.

COUNT II: INFRINGEMENT OF THE '550 PATENT

24. Plaintiff incorporates the preceding paragraphs as if fully set forth herein.

25. On information and belief, STM has infringed the '550 Patent pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, offering to sell, selling in the United States or importing into the United States products incorporating DMA controllers, including the Accused STM Products identified in Attachment A.

26. For example, on information and belief, STM has infringed at least claim 1 of the '550 Patent by making, using, offering to sell, selling in the United States or importing into the United States the STM STM32F100xx Series MCUs, which are computing systems comprising a bus, a

main memory coupled to the bus, and a central processing unit. *See* Ex 7, STM32F100xx reference manual, p. 1 and 143-144. The accused products further comprise a DMA controller that controls direct memory access transfers to and from main memory. *See id.*, 142 ("Direct memory access (DMA) is used in order to provide high-speed data transfer between peripherals and memory as well as memory to memory. Data can be quickly moved by DMA without any CPU actions."). STM's DMA Controllers include a register set for providing control and status of the direct memory access transfers to and from the main memory. *See id.*, 152-159 ("DMA registers"). STM's DMA Controllers provide limited access to registers within the register set, for example, when a channel is enabled. *See id.*, 157-159 (the DMA_CPARx and DMACMARx registers "must *not* be written when the channel is enabled."). STM DMA Controllers include a configuration register having a first control field, wherein access provided to registers within the register set changes based on a value placed in the first control field. For example, "Bit 0 EN: Channel enable" in the "DMA channel x configuration register (DMA_CCRx)" can disable the channel, allowing access to the above registers to be changed, such as allowing the above registers to be written. *Id.* at 154-55.

27. On information and belief, STM has induced, and continues to induce, infringement of the '550 Patent pursuant to 35 U.S.C. § 271(b), by actively and knowingly inducing, directing, causing, and encouraging others, including, but not limited to, its partners, software developers, customers, distributors, and end users, to make, use, sell, and/or offer to sell in the United States, and/or import into the United States, the Accused Products by, among other things, providing instructions, manuals, and technical assistance relating to the integration, set up, programming, use, operation, updates, and maintenance of said products, such as hardware manuals, software manuals, and other technical documentation available on the STM website.

28. On information and belief, STM has committed the foregoing infringing activities without a license.

29. On information and belief, STM's infringing activities commenced at least six years prior to the filing of this complaint, entitling Complex Memory to past damages.

30. On information and belief, STM knew the '550 Patent existed, knew of its claims, and knew of STM's infringing products while committing the foregoing infringing acts, thereby willfully, wantonly, and deliberately infringing the '550 Patent.

COUNT III: INFRINGEMENT OF THE '481 PATENT

31. Plaintiff incorporates the preceding paragraphs as if fully set forth herein.

32. On information and belief, STM has infringed, and continues to infringe the '481 Patent pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, offering to sell, selling in the United States or importing into the United States the Accused STM Products identified in Attachment A.

33. For example, on information and belief, STM infringes at least claim 16 of the '481 Patent by performing a method of accessing data. On information and belief, the Accused STM Products, such as the Telemaco3P family, include and/or access data in DDRxL and LPDDRx memory. *See* Ex. 8, STMicroelectronics Telemaco3P automotive family of telematics and connectivity microprocessor Data Brief ("Memory Interfaces…16-bit-DDR3L-1066…16-bit LPDDR2-800"). The Accused STM Products generate a first access request for accessing data stored at memory locations of a first memory row. *See, e.g.*, Ex. 9 "LPDDR2 Standard, JESD209-2B" at p. 18 ("LPDDR2-S is a high-speed SDRAM device internally configured as a 4 or 8-Bank memory…. Read and write accesses to the LPDDR2 are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. For LPDDR2-SX devices, accesses begin with the registration of an Activate

command, which is then followed by Read or Write command. The address and BA bits registered coincident with the Activate command are used to select the row and the Bank to be accessed. The address bits registered coincident with the Read or Write command are used to select the Bank and the starting column location for the burst access."). The memory locations of the first memory row are disposed upon a substrate. *See id*. The Accused STM Products access the data stored at the memory locations identified in the first access request. *See id*. While the data stored at the memory locations identified by the first access request is being accessed, the Accused STM Products generate a second access request for accessing data stored at memory locations of a second memory row. *See, e.g.*, Ex. 9 at 113 ("NOTE 3 After Read with AP, seamless read operations to different banks are supported. After Write with AP, seamless write operations to different banks are supported."). In the Accused STM Products, the memory locations of the second memory row are also disposed upon the substrate at which the memory locations of the first memory row are disposed. *See id*. The Accused STM Products also access the data stored at the memory locations identified in the second access request. *Id.*

34. On information and belief, STM has induced, and continues to induce, infringement of the '481 Patent pursuant to 35 U.S.C. § 271(b), by actively and knowingly inducing, directing, causing, and encouraging others, including, but not limited to, its partners, software developers, customers, distributors, and end users, to make, use, sell, and/or offer to sell in the United States, and/or import into the United States, the Accused Products by, among other things, providing instructions, manuals, and technical assistance relating to the integration, set up, programming, use, operation, updates, and maintenance of said products, such as hardware manuals, software manuals, and other technical documentation available on the STM website.

35. On information and belief, STM has committed the foregoing infringing activities

without a license.

36. On information and belief, STM's infringing activities commenced at least six years prior to the filing of this complaint, entitling Complex Memory to past damages.

37. On information and belief, STM knew the '481 Patent existed, knew of its claims, and knew of STM's infringing products while committing the foregoing infringing acts, thereby willfully, wantonly, and deliberately infringing the '481 Patent.

COUNT IV: INFRINGEMENT OF THE '576 PATENT

38. Plaintiff incorporates the preceding paragraphs as if fully set forth herein.

39. Upon information and belief, STM has infringed, and continues to infringe, the '576 Patent pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, offering to sell, selling in the United States or importing into the United States the Accused STM Products identified in Attachment A.

40. For example, on information and belief, STM has infringed at least claim 25 of the '576 Patent by performing steps of an energy-conserving operating system. For example, the Accused STM Products include STM's STiH Systems-on-Chip. On information and belief, the STM STiH SoCs include an ARM Cortex-A9 MPCore, and perform the steps of claim 25 of the '576 Patent. *See, e.g.,* Ex. 1, STiH416 Datasheet ("The STiH416 SoC provides high security and system integration, functionalities tailored to both the broadcast and broadband ecosystems, accessibility for open platform software applications, eye-popping performance and unequalled power efficiency.") The Accused STM Products activate a set of keep-alive operating instructions for providing an energy-conserving operation that utilizes keep-alive microprocessor circuitry. For example, STMicro devices activate a set of keep-alive instructions in a "Low Power Processor." *Id.* at 1. If detecting a power-up signal, the Accused STM Products power up to provide a main operation that utilizes main microprocessor circuitry and a set of main

operating instructions. For example, if detecting a power-up signal while in low power or sleep mode, such as a wakeup signal, STM devices power up the main Application Processor (main microprocessor circuitry) which run main operating instructions, such as the Linux kernel, drivers, and applications. *Id.* The Accused STM Products power down to provide said energy-conserving operation in which said main microprocessor circuitry is deactivated, if detecting a power-down signal. For example, if the Accused STM Products detect a power-down signal, such as a software instruction, they power down the Application Processor (main microprocessor circuitry) while the "low power processor" remains alive. *Id.* In the Accused STM Products, said keep-alive operating instructions provide said energy-conserving operation requiring less computation power as compared with said main operating instructions. *Id.*

41. On information and belief, STM has induced, and continues to induce, infringement of the '576 Patent pursuant to 35 U.S.C. § 271(b), by actively and knowingly inducing, directing, causing, and encouraging others, including, but not limited to, its partners, software developers, customers, distributors, and end users, to make, use, sell, and/or offer to sell in the United States, and/or import into the United States, the Accused Products by, among other things, providing instructions, manuals, and technical assistance relating to the integration, set up, programming, use, operation, updates, and maintenance of said products, such as hardware manuals, software manuals, and other technical documentation available on the STM website.

42. On information and belief, STM has committed the foregoing infringing activities without a license.

43. On information and belief, STM's infringing activities commenced at least six years prior to the filing of this complaint, entitling Complex Memory to past damages.

44. On information and belief, STM knew the '576 Patent existed, knew of its claims, and

knew of STM's infringing products while committing the foregoing infringing acts, thereby willfully, wantonly, and deliberately infringing the '576 Patent.

PRAYER FOR RELIEF

WHEREFORE, Complex Memory prays for the judgment in its favor against STM, and specifically, for the following relief:

A. Entry of judgment in favor of Complex Memory against STM on all counts;

B. Entry of judgment that STM has infringed the Patents-in-Suit;

C. Entry of judgment that STM's infringement of the Patents-in-Suit has been willful;

D. Award of compensatory damages adequate to compensate Complex Memory for STM's infringement of the Patents-in-Suit, in no event less than a reasonable royalty trebled as provided by 35 U.S.C. § 284;

E. Complex Memory's costs;

F. Pre-judgment and post-judgment interest on Complex Memory's award; and

G. All such other and further relief as the Court deems just or equitable.

DEMAND FOR JURY TRIAL

Pursuant to Rule 38 of the Fed. R. Civ. Proc., Plaintiff hereby demands trial by jury in this action of all claims so triable.

Dated: November 12, 2018

Respectfully submitted,

/s/ Hao Ni

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ATTACHMENT A

Accused STMicroelectronics, Inc. Products

STiH Systems-on-Chip, including:
STiH301
STiH305
STiH310
STiH312
STiH410
STiH412
STiH418

Telemaco processors, including:
STA1078
STA1079
STA1195
STA1385

STM32 microcontrollers, including:
STM32H7
STM32F7
STM32F4
STM32F2
STM32F3
STM32F1
STM32F0
STM32L5
STM32L4+
STM32L4
STM32L1
STM32L0

Development Boards, Expansion Boards, Discovery Kits, and Evaluation Kits for the above-listed processors and SoCs.